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10/658,977	09/10/2003	Jack C. Wybenga	2003.09.014.BN0	1863

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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,977	WYBENGA ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/658,977** has a total of *22* claims pending in the application; there are *3* independent claims and *19* dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by **Lipman et al. (U.S. Patent No. 6,192,051 hereafter referred to as Lipman)**.

With respect to independent **claims 1 and 11,**

"A router **[Lipman discloses in column 1, line 32, "...high-throughput routers"]** *for interconnecting N interfacing peripheral devices,* **[See FIGs. 1-3. Lipman also discloses in column 6, line 54, "...devices"]** *said router comprising: a switch fabric;* **[column 3, line 19, "...switch fabric"]** *and a plurality of routing nodes* **[column 1, lines 10-12, "...routing of data packets or frames from a source network node to one or more destination network nodes."]** *coupled to said switch fabric, each of said routing nodes comprising: a plurality of physical medium device (PMD) modules* **[column 3, lines 12-19, "a collection of line cards interconnected by a switching fabric. Each line card has one or more ports each attached to a corresponding physical network medium."]** *capable of transmitting data packets to and receiving data packets from selected ones of said N interfacing peripheral devices;* **["...When a packet arrives at a line card port, a forwarding engine on the line card determines which port the packet should be forwarded to, and then forwards the packet to the corresponding line card through the switch fabric."]** *an input-output processing (IOP) module coupled to said PMD modules and said switch fabric and capable of routing said data packets between said PMD modules and said switch fabric and between said PMD modules;* **[FIG. 9, elements 188, 170, 172]** *and a lookup circuit* **["lookup logic", column 5, line 39]** *associated with said IOP module for translating received addresses*

associated with said data packets into destination addresses, **[column 5, lines 19-20, "...unique routing entries associated with the corresponding set of addresses."]** *said lookup circuit comprising M pipelined memory circuits* **[FIG. 10, element 139, "Forwarding Table"]** *for storing a trie table capable of translating a first received address into a first destination address,* **[See FIG. 11]** *wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit."* **[See FIG. 11]**

With respect to **claims 2 and 12,**

"The lookup circuit as set forth in claim 1, wherein said output of said first memory circuit comprises a first address pointer **[See FIG. 11, elements 214, 218, or 222]** *that indexes a start of said address table* **[element 152]** *in said second memory circuit."***[Level 2 Sparse Tree of FIG. 11]**

With respect to **claims 3 and 13,**

"The lookup circuit as set forth in claim 2, wherein said first address pointer **[See FIG. 11, elements 214, 218, or 222]** *and a second portion of said first received address* **[See FIG. 11, element 180]** *access said address table in said second memory circuit."* **[Level 2 Sparse Tree of FIG. 11]**

With respect to **claims 4 and 14,**

"The lookup circuit as set forth in claim 3, wherein an output of said second memory circuit **[See FIG. 11, element 154]** *accesses an address table in a third memory circuit."* **[Level 3 Sparse Tree of FIG. 11]**

With respect to **claims 5 and 15,**

"The lookup circuit as set forth in claim 4, wherein said output of said second memory circuit comprises a second address pointer **[See FIG. 11, elements 214, 218, or 222]** *that indexes a start of said address table in said third memory circuit."* **[Level 3 Sparse Tree of FIG. 11]**

With respect to **claims 6 and 16,**

"The lookup circuit as set forth in claim 5, wherein said second address pointer and a third portion of said first received address access **[See FIG. 11, element 180]** *said address table in said third memory circuit."* **[Level 3 Sparse Tree of FIG. 11]**

With respect to **claims 7 and 17,**

"The lookup circuit as set forth in claim 6, wherein address pointers output from said M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, **[column 5, line 25, "routing table." See FIG. 7]** *said routing table comprising a plurality of destination addresses associated with said received addresses."* **[column 5, lines 19-20, "...unique routing entries associated with the corresponding set of addresses." Also see column 10, lines 33-38]**

With respect to **claims 8 and 18,**

"The lookup circuit as set forth in claim 7, further comprising a memory interface **[column 14, line 55, "address resolution memory"]** *capable of selectively applying to said final memory circuit an address pointer* **[column 14, line 56, "level/base pointers"]** *associated with said first received address* **[See FIG. 11]** *and an address pointer associated with a subsequently received address,* **[See FIG. 11]** *such that said address pointer associated with said first received address is applied to said final memory circuit prior to said address pointer associated with said subsequently received address."* **[FIGs. 12-14]**

With respect to **claims 9 and 19,**

"The lookup circuit as set forth in claim 8, wherein said M pipelined memory circuits **[FIG. 10, element 139, "Forwarding Table"]** *comprise static random access memory (SRAM) circuits."* **[column 14, line 58, "RAM 188" See FIG. 9, element 188. It is notoriously well known to use static RAM as a form of RAM]**

With respect to **claims 10 and 20,**

"The lookup circuit as set forth in claim 9, wherein said final memory circuit comprises a dynamic random access memory (DRAM) circuit." **[column 14, line 58, "RAM 188" See FIG. 9, element 188. It is notoriously well known to use dynamic RAM as a form of DRAM]**

With respect to independent **claim 21,**

"A method for translating a first received address into a first destination address **[column 5, lines 19-20, "...unique routing entries associated with the corresponding set of addresses." Also see column 10, lines 33-38]** *using M pipelined memory circuits that store a trie table,* **[FIGs. 10, element 139, "Forwarding Table" and FIG. 15. Also see "Patricia Tree" in column 3, line 3]** *the method comprising the steps of: accessing an address table in a first memory circuit using a first portion of the first received address; outputting from the address table in the first memory circuit a first address pointer that indexes a start of an address table in a second memory circuit; and accessing the address table in the second memory circuit using the first address pointer and a second portion of the first received address."* **[This method is disclosed by Lipman in FIGs. 12-14]**

With respect to **claim 22,**

"The method as set forth in claim 21 further comprising the steps of: outputting from address table in the second memory circuit **[FIGs. 12-14, element 232]** *a second address pointer* **[FIGs. 12-14, element 234]** *that indexes a start of an address table in a third memory circuit;* **[FIGs. 12-14, element 272]** *and accessing the address table in the third memory circuit* **[FIGs. 12-14, element 276]** *using the second address pointer and a third portion of the first received address."* **[This method is disclosed by Lipman in FIGs. 12-14]**

CONCLUSION

Status of Claims in the Application

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i):**

Claims rejected in the Application

Per the instant office action, claims **1-22** have received a first action on the merits and are subject of a first action non-final.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status

information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner

Art unit: 2189

DONALD SPARKS
SUPERVISORY PATENT EXAMINER